Still a Tale of Two Paths:

Highlights of Lithography Panel from SEMICON West 2013

Vivek Bakshi, EUV Litho, Inc.

July 21, 2013

This year I moderated the industry's Lithography Panel during SEMICON West 2013 to a standing room only crowd. This interest in Litho was not a surprise. As it was pointed out by keynote speaker Ajit Manocha, CEO of GlobalFoundries, at 20 nm lithography equipment now comprises 85% of the cost of a new fab. This is up from 70% at 90 nm! So if you look at all those booths on the floor of SEMICON West 2013, ASML and Nikon are doing 85% of the new fab business. That is huge as ASML is getting most of that 85% share and their share is growing. Overall, one can see lot of interest in understanding what is next in the world of lithography, as that is a big chuck of the semiconductor business and Litho is the key enabler of Moore's Law.

Currently, both 193 immersion multiple patterning (193i MP) and EUV Lithography (EUVL) are the leading contenders for next generation lithography for the 10 nm node and below. The SEMICON West 2013 panel was great as we had speakers on both 193i MP (Nikon and Synopsys) as well as EUVL (SEMATECH and ASML). TEL talked about directed self assembly (DSA) applicable to both approaches. Nowadays all large workshops and symposia have separate tracks that focus on one or the other, so it was good to have both of them together. The title of the lithography panel was "Still a Tale of Two Paths" and both sides essentially talked about the merits of their own approach and issues with the other's approach. (ASML makes both EUVL and 193i scanners while Nikon makes only 193i scanners. Synopsys supports both approaches via their modeling software and TEL makes tracks for both types of scanners.)

The lithography session underscored the issues that we are having in the search for next generation lithography (NGL) technology. There were "two elephants" in the room that all speakers tried to ignore: 1) the cost, complexity and possible technical impossibility of 193i MP below 10 nm, and 2) delays for EUVL due to lack of source power. The "elephants" were not discussed but their presences were very much felt. 193i MP is getting very expensive and complicated and may not be able to support patterning below the 10 nm node without additional complexity that chipmakers are not willing to adopt. EUV lithography right now still remains in the pilot line due to lack of adequate power. Hence, if scaling required by Moore's Law is no longer supported

soon, there will be an historic cost increase. Before I give my opinion on what I think may happen, let me first summarize what I heard from speakers and otherwise at SEMICON West 2013.

Talk Summary

Nikon titled its first talk “EUV Revolution Has Been Postponed” and then described how to move forward with 193i MP. It is the most probable route if EUVL is absent in HVM to provide resolution scaling, control of CD uniformity and overlay, and flexibility with design and cost. However, it is known that flexibility is reduced in MP with design restrictions and I pointed out during Q & A that Nikon’s comparison of MP with EUVL was not correct. The cost for 193i MP must include all equipment needed to support this technique. A scanner in MP is not just a scanner but a “large composite tool” that contains tools for deposition, etch, ash and metrology, and cost of all these must be included. However, in the absence of EUVL in HVM, 193i MP remains the main choice for chip makers.

In the next talk, Stefan Wurm of SEMATECH pointed out the readiness of EUV resists for EUVL introduction. EUV resists have been ready in part due to the testing infrastructure provided by SEMATECH and other consortia. His consortium is now focused on getting EUV mask blanks ready for HVM introduction of EUVL. The next set of challenges is to reduce pits, bumps and scratches in the substrate, focus on mask lifetime issues during cleaning and handling and reduce damage of backside coatings. In response to a question, Stefan pointed out that an EUVL mask should be able to go through 100 clean cycles, compared to today’s performance of 30 to 40 cleans.

Skip Miller of ASML presented data on the progress of EUVL scanners. He reported the shipment of two NXE3300B scanners to customers. He pointed out 30-70% lower cycle time via EUVL scanners compared to 193i based scanners and a large process window for 14 nm node and below. He also pointed out that at 10 nm node EUVL allows 50% scaling, while only 25% is possible with 193i MP. Even for grided SRAM chip makers will prefer EUVL, as limited overlay makes MP very difficult. For NXE3300B, throughput targets are 50-125 WPH, based on indications that his power vs. throughput curve will correspond to 68 - 250 W of source power. Currently 40-50 W of sources have been run with good dose repeatability of <0.5% for total run time of 20 hours, consisting of many hourly runs. I am not sure if runs were at 100% duty cycle. The target for these scanners in 2014 is for 70 WPH, and he expects 250 W source power to be achieved in 2015.

Mike Rieger of Synopsys gave described the role of electronic design automation (EDA) in enabling scaling via 193i MP. Scaling is possible without EUVL but will entail increasing cost, process complexity and design rules restriction. He pointed out need to keep cost under control for these options.

Ben Rathsack of TEL presented collaborations in the area of directed self-assembling (DSA), an emerging technology area that can help 193i MP as well as EUVL. He described his collaboration efforts in the area of defect reduction metrology via continued research with universities and consortia as well as chip makers.

The EUV revolution has not been postponed – it is delayed. The advantages of EUVL due to relaxed k1 and cost competitiveness are well known to chipmakers and what they want are tools that can support HVM, and those are delayed due to low source power.

Industry's Position and Critical Questions

"Lithography is one of the highest priorities of our industry" and "EUVL must happen" were some of the comments we heard from consortia leaders at SEMICON West in other panel discussions in the meeting. These industry consortia have a combined budget of few hundred million per year and most of it is focused on EUVL. They have done a wonderful job of supporting mask and resist research. As they are funded by chipmakers and some government support, one can assume the view of the consortia is the position of chipmakers as well.

"Suppliers will deliver the EUV sources" has long been repeated by all consortia and they reiterated their position in this meeting as well. Currently consortia support all but EUV source projects, while EUVL continues to slip due to lack of adequate source power. In the end it is the chip makers who pay for the delay and the consortia reflect their strategy, so one wonders why this is so. Perhaps human psychology it is at work here. People do what they are comfortable doing and generally avoid trying new things unless calamity strikes. Mask and resist is something chip makers know how to deal with and have experience in developing these technologies. However, they do not have a team of plasma experts or source experts to guide them. Neither do consortia, so one has to go with what suppliers can provide. It is interesting that we are ready to bet the future of Moore's Law rather than do something to hedge our risk. Year after year source power roadmaps slip, but no additional action is taken except to wait for new supplier source power roadmaps that we know will slip again.

Some point out to me is that the critical question today for the industry is, “If EUV Sources will be ready, will mask infrastructure be ready?” I agree that this is an important point and will address it below briefly. However, I think the most important question is, “What we will do with ready EUVL masks and EUV resists, if sources delay EUVL sufficiently to push it out further on roadmaps?”

EUVL mask infrastructure challenges (as detailed in the 2013 EUVL Workshop by Intel, Toshiba and GlobalFoundries) are certainly very difficult but do not look like showstoppers. They can be addressed with significant efforts and investment. What is lacking in the mask area is the consensus on key topics such as choice for masks for High NA tools, need for pellicles, how to inspect patterned masks during manufacturing, and need for various mask metrology tools during manufacturing, usage and maintenance of masks. Mask defect metrology tools are still not ready mostly due to lack of high brightness (not high power) EUV sources. In the upcoming 2013 Source Workshop, I expect more discussions and ideas presented on how to advance source technology for metrology sources.

My Predictions

I may be biased toward EUVL, but 193i MP will get more expensive and complex than EUVL at every next node, but EUVL is not yet ready so chip makers have no choice but to go with what is available. ASML announced in their presentation that two NXE3300B tools have been shipped and nine more are on their way to chipmakers. I think 50 W sources will be ready and working in NXE3300B sometime in 2014, corresponding to 43 WPH throughput. 100 W sources will be ready in 2015 or 2016 corresponding to 73 WPH. The readiness of 250 W EUV sources cannot be safely predicted, unless we see 100 W sources ready and have identified the issues to ensure that they are no showstoppers. I am not convinced that present approaches can get to 500 W sources. It is easy to put them on roadmaps, but delivering them is another question.

With 73 WPH, one can start with EUVL in HVM, as that cost is going to be better than for multiple pattering. Below 10 nm nodes, the cost for 193i MP is high due to 4x or 8x patterning and for EUVL due to lower throughput due to low source power. I am not as concerned about 450 mm transition for EUVL tools. EUV sources will have to deliver 2.5 x source power to keep the same throughput as 300 mm tools, and that does not seem to be out of question by 2018, when the competition will be 4x patterning with extreme design rule limitation.

Another question to ask is how far you can scale with 193i MP and what are the cost implications. If EUVL is still not ready in few years and 193i MP is not feasible due to cost and complexity, what do we do?

Both are projection lithography and rate of transfer of information from mask to wafer cannot be beaten by direct write techniques? This topic needs continued discussion.

Epilogue

Getting out of SEMICON for my next meeting, I was stopped by a colleague, who reminded me that EUVL was dead. Of course, he has been telling me the same thing since 2006, even while his own NGL approaches have gone bust. It appears that industry has been split into pro- and anti-EUVL camps for some time. It is becoming something like a religious war and there is less of a dialogue between these two camps. EUVL has been proven to be capable but it is delayed and will not be ready for HVM for a few more years. 193i MP is getting to be very complicated and expensive so chip makers have to have a backup, and that is EUVL. In the end it may be a mix of EUVL and 193i MP that will enable continuation of feature size scaling. The industry must continue to follow Moore's Law and will do whatever it takes to keep up the scaling, so NGL will remain a hot topic for many years to come.